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Original article

Low Power, Low Area Digital Modulators using Gate Diffusion Input Technique

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ABSTRACT

Audio playback devices like IPODs and MP3 players use Sigma Delta Digital to Analog Converters (DACs) where the size and power consumption is of prime importance. Digital modulator is the most important part of Sigma Delta DACs. This paper presents a new approach for the implementation of a sample digital MASH 1-1 and MOD 2 modulator using Gate Diffusion Input (GDI) technique. The same modulators are also implemented in standard CMOS technology and are compared for the tone frequencies of the audio frequency range. The proposed modulators using GDI method provide a significant improvement in the area, power, and power delay product as compared to CMOS. The gate level simulation using WinSpice with 0.18 μm technology confirms the usefulness of the presented structures.

1. Introduction

In the era of digital communication, Analog to Digital Converters (ADCs) and Digital to Analog Converters (DACs) play crucial roles. Nyquist-rate DAC or an oversampling DAC can be used depending upon resolution, application, and technology. Low bandwidth, high-resolution applications like Audio, uses oversampling DACs. In these DACs, the complexity of digital circuits is more, but the analog reconstruction filter required is of lower order and has broad transition band. The area and complexity of such DACs are directly related to its input word length. The Sigma Delta Modulator is used to reduce the actual word length of these DACs. The various types of Sigma Delta architectures are available: Single Stage Loops, Error Feedback Structures, Multi-stAge noise SHaping (MASH) structures. Noise shaping performance of a single stage modulator increases with the increase in order but reduces the stability. MASH modulators instead provide stability of lower order single stage modulator and noise shaping performance of higher order single stage modulator (Schreier and Temes, 2005).

An advancement of VLSI technology has led to increasing in the requirement of area and power reduction of DACs and ADCs. Some techniques have been proposed to reduce the hardware requirements of MASH modulators. The authors used long word length for the first modulator in MASH structure and shorter word lengths for subsequent stages, thereby reducing the hardware as compared to conventional MASH structure (Ye and Kennedy, 2004). The error masking technique reduced the device consumption of digital MASH modulators and experimental demonstration constructed on Xilinx Spartan 2E FPGA (Ye and Kennedy, 2007). Brian Fitzgibbon, et al. proposed bus splitting methods for hardware reduction for MASH and Error Feedback Digital Delta-Sigma Modulators (Fitzgibbon et al., 2011, 2012). The same authors suggested optimum word lengths of nested digital MASH Sigma Delta Modulator which allowed hardware complexity reduction (Fitzgibbon et al., 2010). in Jerng and Sodini (2007) proposed an area efficient digital second order MASH RF modulator for the wide-band system. The adders and flip-flops were implemented using nMOS pass-gate logic in 0.13 μm technology which generated the power, and area efficiency. Yao and Hsieh (2009) focused on delta path of MASH 1-1-1 Delta-Sigma modulator. By recoding the 1-bit carry output signal from the accumulator as -1′s there was a reduction in hardware complexity of Delta path.

Gate Diffusion Input (GDI) is a new technique for low power digital combinational circuit design. This method provided a

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reduction in power consumption, propagation delay, and area of digital circuits while the logic design complexity was small (Morgenshtein et al., 2002). GDI methodology allows implementation of a wide range of complex logic functions using only two transistors. GDI based design of Arithmetic Logic Unit has been implemented and compared with nMOS pass transistor logic and conventional CMOS techniques. The results show that design using GDI provides lower power consumption, less delay while maintaining the low complexity of logic design (Kumar et al., 2011). Also, a low power and area efficient design of non-overlapping clock generator using GDI based D flip- flops have been implemented (Hari and Mai, 2011). Asynchronous digital circuits like dynamic and SR latch circuits perform better regarding power, area, and speed as compared to CMOS circuits (Morgenshtein et al., 2004a). The authors presented GDI based full adder showing better performance in terms area, power and speed (Uma et al., 2014; Foroutan et al., 2014).

GDI is a new technique for digital circuits implementation with a lot of advantages over existing ones. Therefore, this investigation presents a new approach for the implementations of a sample MASH 1-1 and also a simple MOD 2 modulator for audio frequencies using the GDI technique. The same modulators are also implemented using the standard CMOS technique to justify the usefulness of GDI technology. This analysis also discusses, in brief, the ADC, DAC and Low Pass Filter (LPF) used for the performance evaluation of the modulators. This work analyses the performance of digital modulators regarding Signal-to-Noise-Ratio (SNR), Signal-to-Noise-and-Distortion-Ratio (SNDR), Spurious-Free-Dynamic-Range (SFDR) and, Effective Number Of Bits (ENOB). The key contributions of this work are a new approach for implementation of MASH 1-1 and MOD 2 modulators using GDI technique that offers area reduction, power reduction and reduction in Power Delay Product (PDP) as compared to an implementation using CMOS technology. This work also proposes a new XOR gate implementation using GDI method which requires eight fewer transistors as compared to CMOS technology.

Organization of this paper is as follows: Section 2 discusses the design of both the MASH 1-1 and MOD 2 modulators. Section 3 highlights the design of Linear Ramp ADC, R-2R ladder DAC, and Butterworth Filter. Section 4 discusses the implementation of the modulators along with the performance review. Section 5 presents Simulation Results, and finally, Section 6 summarizes the Conclusions of the work.

2. Digital modulators

Fig. 1(a) shows the block diagram of Sigma Delta DAC. The basic blocks of Sigma Delta DAC are interpolation filter, modulator, the internal DAC and analog reconstruction filter. The complete block diagram of Delta Sigma DAC implemented in this work is as shown in Fig. 1(b). It consists of Linear Ramp ADC at the input side and R-2R Ladder DAC along with fourth order Butterworth LPF at the output end. Instead of an interpolation filter at the input of Sigma Delta DAC, the ADC was designed to generate digital data stream sampled at $OSR \cdot F_s$, where OSR is Over-Sampling Ratio, and F_s is Nyquist sampling frequency.

The modulators used in this work are a two stage MASH 1-1 modulator with 8-bit input and 4-bit output as shown in the Fig. 2(a) and an error feedback second order modulator MOD 2 with 8-bit input and 4-bit output as shown in Fig. 2(b).

2.1. MASH 1-1 modulator

In the basic equation of MASH modulator

$$V = STF_1 \cdot STF_2 \cdot U - NTF_1 \cdot NTF_2 \cdot E_2 \quad (1)$$

STF_1, STF_2 are the signal transfer functions of first and second stages respectively, NTF_1, NTF_2 are the noise transfer functions of first and second stage respectively. U represents the input to the modulator; V represents the output of modulator and E_2 is the second stage quantization error. In the MASH 1-1 modulator, both the stages are first-order error feedback structures. STF_1 and STF_2 are both z^{-1} whereas NTF_1 and NTF_2 are $(1 - z^{-1})$. The digital filter stages at the output of the modulator loops are designed to cancel the quantization error generated by the first stage such that first stage filter = STF_2 and second stage filter = NTF_1 (Schreier and Temes, 2005). The overall output of the MASH 1-1 modulator is then written as:

$$V(z) = z^{-2} \cdot U(z) - \left(1 - z^{-1}\right)^2 \cdot E(z) \quad (2)$$

Thus, the noise shaping performance is that of a second order single loop converter while the stability is that of first order loop.

Blocks 1 and 2 of Fig. 2(a) are the first order feedback structures; Block 3 represents post filter of Stage 1, and Block 4 is the post filter of Stage 2. Block 1 consists of an 8-bit full adder and 6 D flip-flops acting as delay devices. Block two consists of a

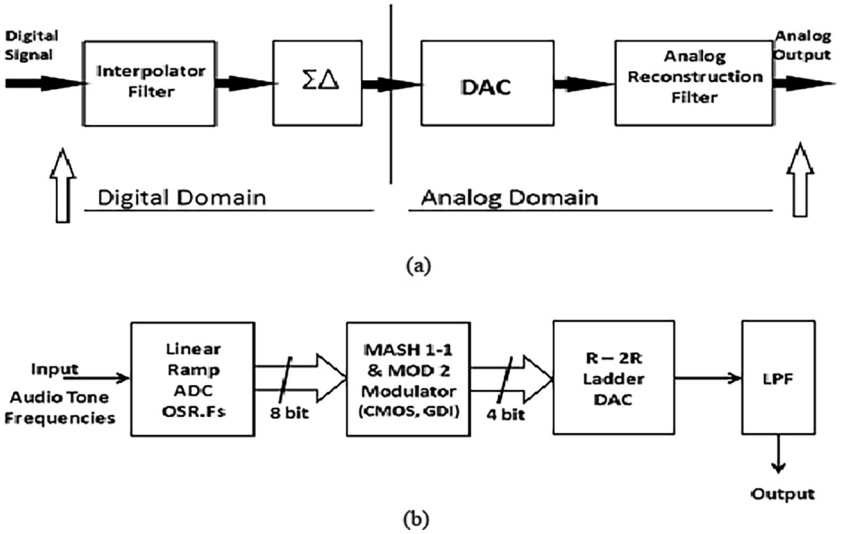

Fig. 1. (a) Block Diagram of Delta Sigma DAC, (b) Implemented Block Diagram of Delta Sigma DAC.

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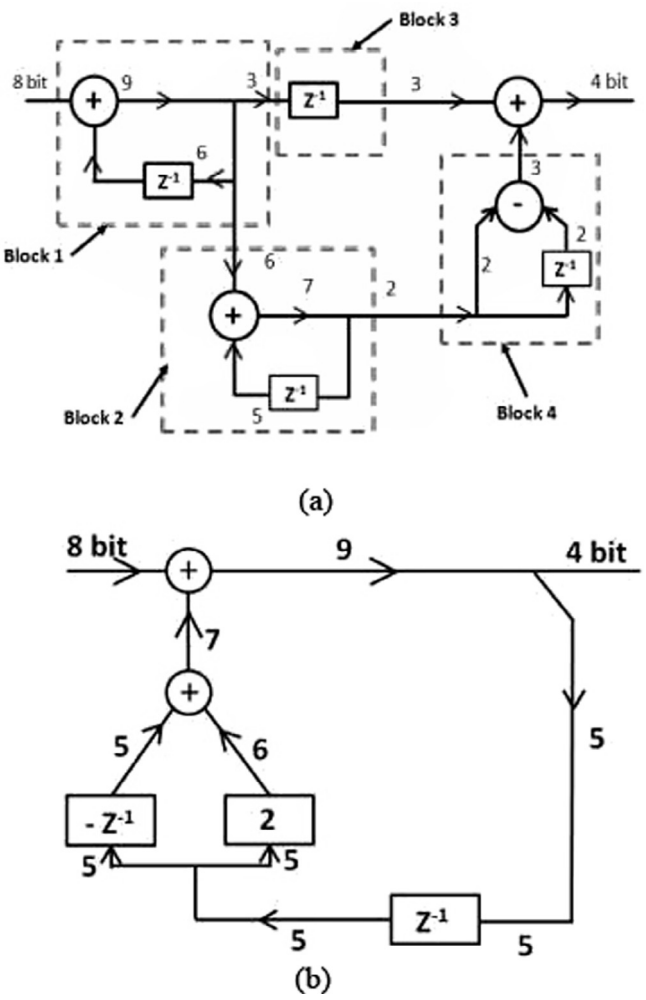

Fig. 2. (a) MASH 1-1 Modulator, (b) MOD 2 Modulator.

6-bit full adder and 5 D flip-flops. Block 3 has 3 D flip-flops whereas Block 4 consists of a 2-bit full subtractor and 2 D flip-flops. 8-bit full adder generates nine output bits (including the carry bit). The adder at the output end is three bit and generates a four-bit output which then acts as input to 4 bit R-2R Ladder DAC. Similarly, 6-bit full adder generates seven output bits, and 2-bit subtractor generates three output bits (including the borrow bit).

2.2. MOD 2 modulator

Using the equation for error feedback structure

$$V(z) = U(z) + [1 - H_e(z)]E(z) \tag{3}$$

where U(z) is the input to the modulator, V(z) is the output of the modulator, E(z) is the truncation error, and $H_e(z)$ is the loop filter used to filter E(z). For a second order modulator,

$$H_e(z) = 1 - \left(1 - z^{-1}\right)^2 = z^{-1}\left(2 - z^{-1}\right) \tag{4}$$

Thus, the MOD 2 modulator is realized using two delays, a multiplier, and two adders as shown in Fig. 2(b). An adder at the input end is an 8-bit full adder with 9-bit output; two 5-bit delay devices were implemented using D flip-flop. Multiplication was performed using D flip-flops and one more full adder with 5 and 6 bit inputs generated 7-bit output. The 4-bit output produced then acts as input to 4-bit R-2R ladder DAC.

The full adders for both the modulators were constructed using 1-bit full adder. Similarly, 2-bit full subtractor was built using 1-bit full subtractor. The positive edge triggered D flip-flop has been built using NAND gates. In CMOS technology, the basic gates were built using push-pull technique and derived from the universal gate.

2.3. GDI technique and full swing XOR gate

In this work, GDI technique was also used to build MASH 1-1 and MOD 2 modulator shown in Fig. 2. The GDI is a new technology used for the design of digital circuits. This method uses the model of a simple cell as shown in the Fig. 3(a). The GDI cell consists of three inputs:

- G-common input to gate terminals of pMOS and nMOS.
- P- input to source or drain terminal of pMOS
- N- input to source or drain terminal of nMOS

VDD and GND are connected to the body of both pMOS and nMOS respectively (Morgenshtein et al., 2002, 2010). The basic gates AND, OR, and XOR generated using single cell produce reduced voltage swing at their outputs due to threshold drops. These drops may cause performance degradation of the entire circuit due to reduced current drive. Therefore, in this work full swing GDI methodology was employed with an addition of a single swing restoration transistor for AND, and OR gates (Morgenshtein et al., 2014). The total number of transistors required for implementing full swing GDI based two input AND and OR gates were 5. The same

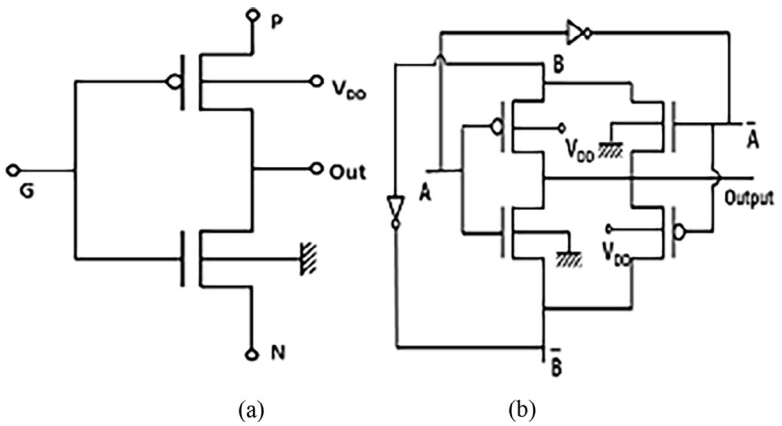

Fig. 3. (a) Basic GDI Cell, (b) Full Swing XOR gate.

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GDI technique had been used to generate full swing XOR gate. Fig. 3(b) illustrates full swing XOR gate. The total number of transistors required for full swing two input XOR gate was eight as is shown in Fig. 3(b). The implementation of inverter needed two transistors in this technique. The GDI based D flip-flop presented, showed improvement in the gate area, the number of devices used, delay and power dissipation as compared to other methods (Morgenshtein et al., 2004b). Due to reduced voltage swings at the output, the D flip-flop mentioned above was not suitable for the current work. Also, the GDI method has no additional advantage regarding transistor count for the universal gates NAND and NOR (Morgenshtein et al., 2014). As a result, D flip-flop implementation remains same as that of CMOS technology.

3. ADC, DAC and Low Pass Filter for the digital modulators

This work also includes the design of ADC at the input end of the digital modulator, DAC and Low Pass Filter (LPF) at the output end of the modulator. Due to the limitation of a maximum number of nodes allowed in WinSpice software, instead of the interpolation filter, ADC itself was designed to generate oversampled output data. $OSR{\cdot}F_s$ was the sampling rate of ADC which produced an 8-bit digital data stream, where OSR = 4.

A large number of ADC architectures are available. Flash designs suffer from significant power dissipation and large area. Pipelined architectures are harder to design. Successive approximation structures are easier to design, but their area increases as large dynamic range and excellent linearity are required. Ramp models are easier to design and have been widely used in front end ASIC for two decades (Delagnes et al., 2007). In Sigma Delta converters, a Sigma Delta ADC at the input side is the correct choice, but as the emphasis of this work was on the modulators, this work used a simple linear ramp ADC (Bell, 2001) as shown in Fig. 4.

Op-amp A1 was designed as a two stage operational amplifier with Miller compensation. It works with supply of 8 V and ground, open loop gain A_{OL} of 800 V/V, Unity Gain Bandwidth (UGB) of 10 MHz, Power Dissipation of 240 μW, Slew Rate of 10 V/μs and Common Mode Rejection Ratio of 50 dB. The operational amplifier A1 used here is in buffer configuration with 160 kHz as the maximum frequency applied which is well below UGB value. Op-amp A2 was designed as a comparator with three stages. The comparator works with supply of 8 V and ground, gain of 1,75,000 V/V, the propagation delay of 9 ns and power dissipation of approximately 800 μW (Baker, 2010).

Many different types of DAC architectures are also available. Current steering DACs offer high performance regarding linearity and high resolution but suffer from low conversion speed. On the other hand, Thermometer DACs provide high conversion rates but require a significant area and power dissipation. R-2 R Ladder DACs have the advantage of ease integration onto small silicon area as they need low device count (Karadimas et al., 2006). Switched

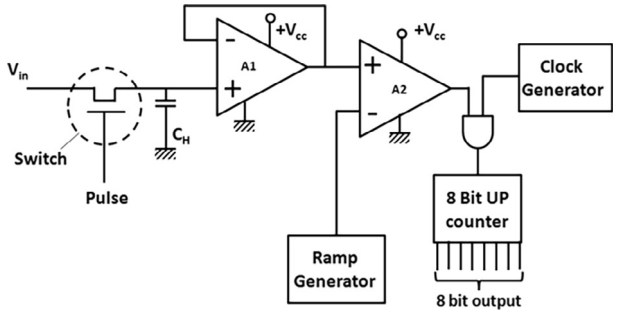

Fig. 4. Block diagram of Linear Ramp ADC.

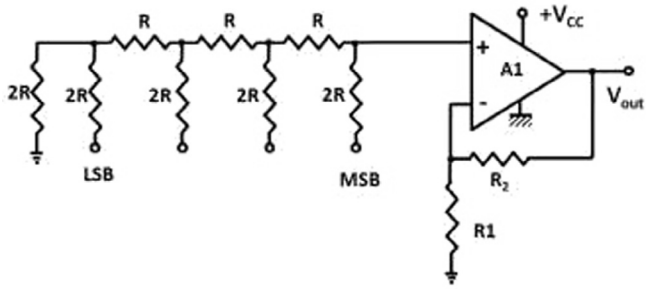

Fig. 5. R-2R Ladder DAC.

capacitor DACs are the internal DACs used in Sigma Delta converters, but as the primary focus of the work was the implementation of digital modulators, this work used a 4-bit R-2R ladder DAC as shown in Fig. 5.

The operational amplifier A1 designed has same specifications of Op-amp A1 in Linear Ramp ADC. The DAC has the same gain for all the input frequencies for both the MASH 1-1 and MOD 2 modulators implementation.

In Sigma Delta converters, Oversampling DACs require an analog smoothing filter whose order should be at least one greater than that of noise shaping (Jons and Martin, 1997). The modulators designed in this work were MASH 1-1 and MOD 2; both provide second order noise shaping. As a result, third order Butterworth low-pass filter would be appropriate, but two extra components provide better noise shaping. Therefore, this work used a fourth order Butterworth LPF as shown in Fig. 6.

The operational amplifiers A1 and A2 of the low pass filter have the same specifications as that of operational amplifier A1 in Linear Ramp ADC. The filters were designed using Sallen and Key unity gain structure (Schaumann and Van Valkenberg, 2001). The component values were calculated from the following equations:

$$A = 1 \text{ and } R1 = R2 = R \tag{5}$$

$$f_H = 1/\left(2\pi R\sqrt{C1C2}\right) \tag{6}$$

$$C_1 = \frac{2}{\propto} \tag{7}$$

$$C_2 = \frac{\propto}{2} \tag{8}$$

where A is the gain of each stage of LPF, f_H is the cut-off frequency of each stage of LPF, α is the damping factor of the LPF, R, C1, C2 are the LPF components.Fig. 7(a) above shows the input of 10 kHz frequency applied to ADC. Fig. 7(b) illustrates the output of LPF with only ADC, DAC and LPF simulated together. Fig. 7(c) and (d) shows LSB and MSB of ADC output which were connected as inputs to DAC. Till date development of only digital circuits was carried out

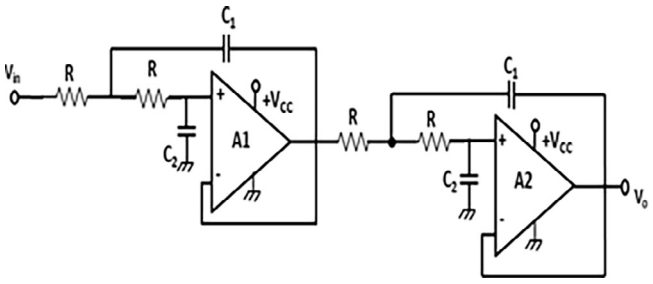

Fig. 6. Fourth order Butterworth LPF.

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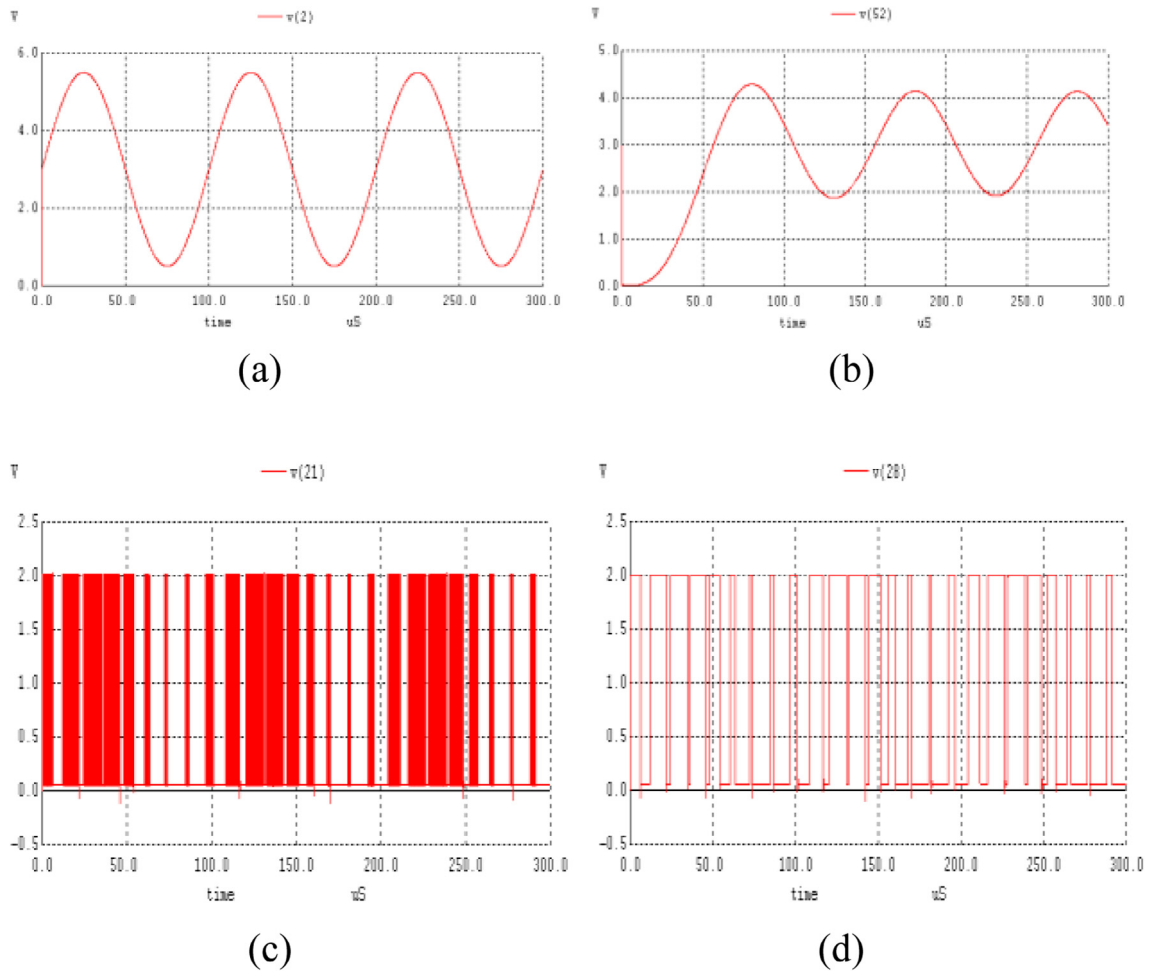

Fig. 7. (a) Input 10 kHz frequency to ADC, (b) Output of LPF, (c) LSB of ADC for 10 kHz frequency, (d) MSB of ADC with 10 kHz frequency.

using the GDI technique and so the ADC, DAC, and LPF developed here were implemented using CMOS technology.

4. Implementation and comparison with the state-of-the-art method

The simulation of both the modulators was performed in WinSpice simulation software using 0.18 μm technology. Implementation of NAND and NOR gates using GDI method does not provide any advantage over standard CMOS technology. As a result, the number of transistors required for D flip-flop implementation using three input NAND gate remains same.

Table 1
Number of transistors per Gate.

Gate	CMOS Technique	Full Swing GDI Technique
2 Input AND	6	5
2 Input OR	6	5
2 Input XOR	16	8
Inverter	2	2
3 Input NAND	6	6

4.1. Implementation of the modulators

Table 1 shows the number of transistors needed for implementing each gate using CMOS and GDI (full swing) method. Due to full swing GDI method used, the number of transistors required for implementing AND and OR gate is five as compared to the two transistors needed to gates implemented using basic GDI technique. The empirically found Width/Length (W/L) of pMOS transistors was 10.8 μm/1 μm, and nMOS transistors was W/L = 7.2 μm/1 μm for MASH 1-1 modulator using both the technologies. The W/L found for pMOS was 3.6 μm/1 μm, and nMOS was 2.4 μm/1 μm for MOD 2 modulator in both the technologies. The calculation of area for the single transistor was performed directly by using W * L. Table 2 reflects the total area required by MASH 1-1 and MOD 2 modulators using the two techniques. As the circuit contains delay devices in the feedback of adders/subtractors, the

Table 2
Simulated Results of MASH 1-1 and MOD 2 using CMOS and GDI Technique.

Technique	Area (μm^2)		Power (μW)		Delay (μs)		PDP (pJ)	
	MASH 1-1	MOD 2	MASH 1-1	MOD 2	MASH 1-1	MOD 2	MASH 1-1	MOD 2
CMOS	13770	3216	23	2.1	0.58	0.3	13.3	0.63
GDI	10487	2410	14	1.6	0.8	0.3	11.3	0.48

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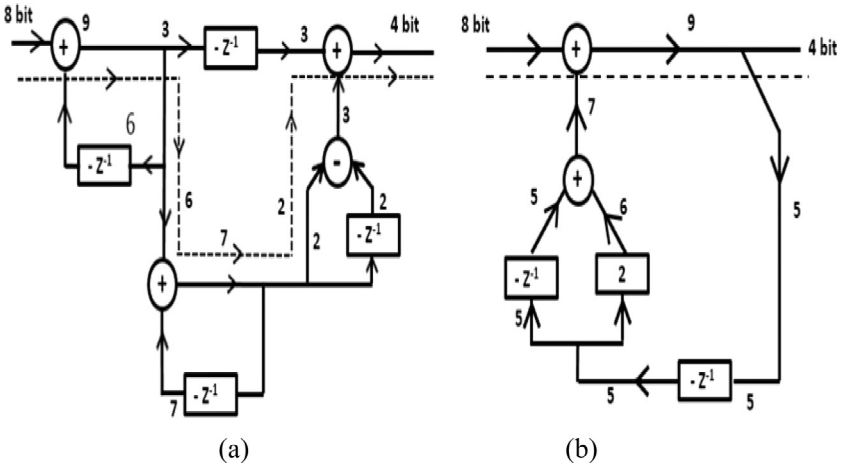

Fig. 8. (a) Path for calculating propagation delay of MASH 1-1, (b) Path for calculating propagation delay of MOD 2.

calculation of propagation delay was done using the path as shown in the Fig. 8. The calculation of propagation delay was obtained by asserting clear to all flip-flops and deactivating the clock. The proposed full swing GDI based MASH modulator generates more delay as compared to CMOS based modulator whereas the delay remains same for MOD 2 modulator. Table 2 mentions the achieved propagation delays.

The calculation of the average power which is sum of dynamic and static power dissipation of the circuits was performed according to the power meter discussed Kang and Leblebici (1999). Both the modulators work with 2 V supply voltage with a load capacitance of 10 fF at the maximum frequency of 160 kHz. Table 2 shows calculated the average power and PDP.

4.2. Performance measures

Data converter performance measures were used to show that the proposed MASH 1-1 and MOD 2 using GDI technique performs similarly to the one using CMOS technology. The most general data converter performance indicators are SNR, SNDR, SFDR, and ENOB which were used here (Janssen and van Rermund, 2011; Balestrieri et al., 2006; LeCroy Corporation, 2011). Following equations were used to calculate the performance parameters:

$$SNDR = 20 * \log\left(\frac{Fundamental}{\sqrt{Noise^2 + Harmonics^2}}\right) \quad (9)$$

$$SNR = 20 * log\left(\frac{Fundamental}{\sqrt{Sum(Noise)^2}}\right) \quad (10)$$

$$SFDR = 20 * \log\left(\frac{Fundamental}{Highest\ Spurious}\right) \quad (11)$$

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad (12)$$

The input to both the modulators using CMOS and GDI techniques was tone frequencies of the audio frequency range. The sample tone frequencies used were 3 kHz, 5 kHz, 10 kHz, 15 kHz, and 20 kHz. The number of nodes in the entire circuit of MASH 1-1 using CMOS technique (ADC, Modulator, DAC and LPF) were 1218 whereas for MASH 1-1 using GDI technology they are 971. For 3 kHz frequency, one cycle is 333 μs. For simulation purpose, at least two cycles of 3 kHz should be used. As a result with 1218 nodes and 666 μs simulation time, personal computer's memory was not sufficient to carry out the full simulation. So, readings were not completed for 3 kHz frequency applied to MASH 1-1 modulator using CMOS. For Sine wave excitation to ADC, Fig. 9.

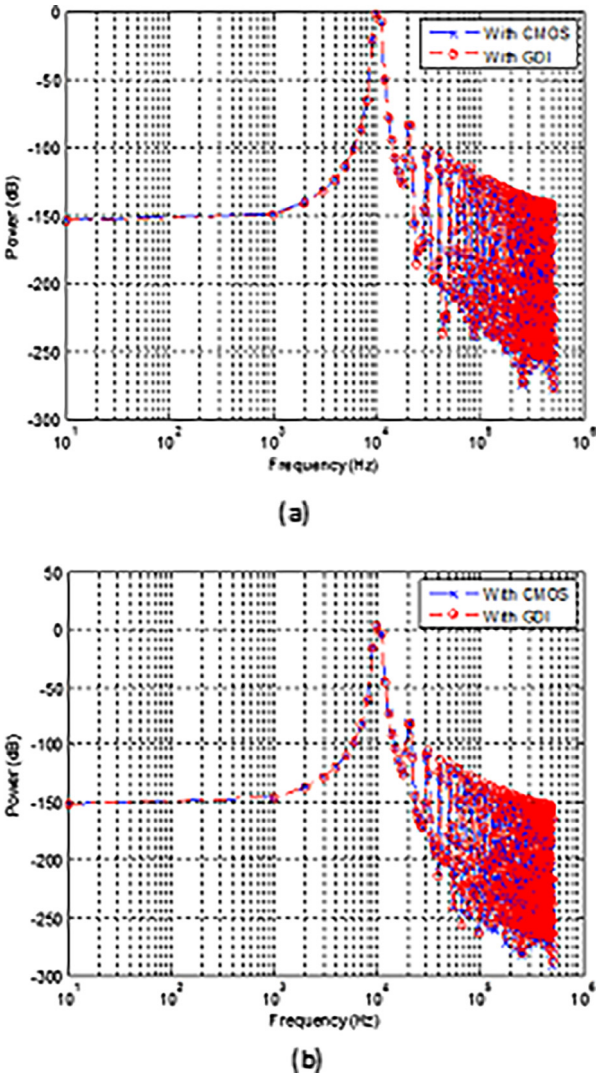

Fig. 9. (a) Output Power Spectrum of 10 kHz CMOS and GDI based MASH 1-1 with DC removed, (b) Output Power Spectrum of 10 kHz CMOS and GDI based MOD 2 with DC removed.

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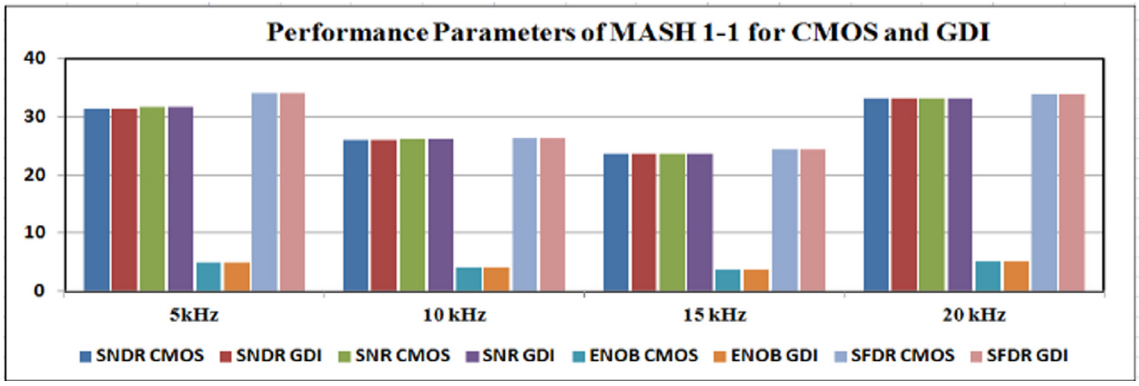

Fig. 10. Comparison of Performance Parameters for MASH 1-1.

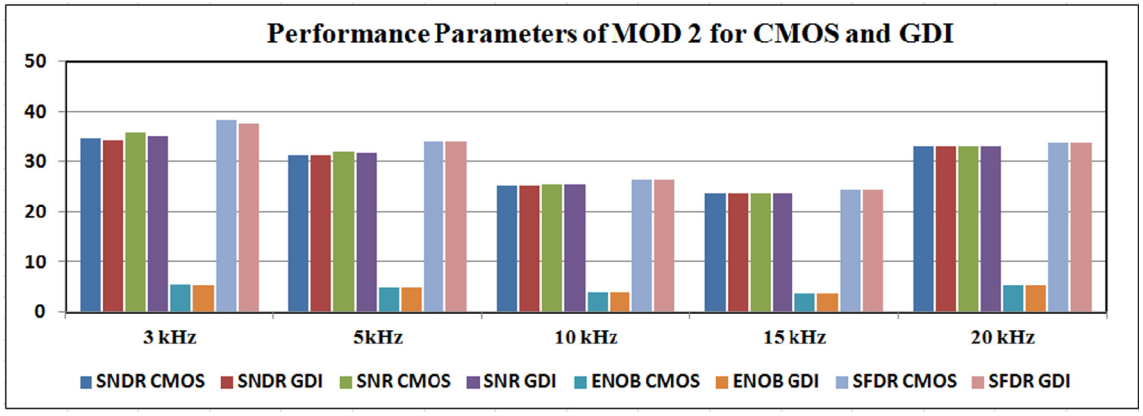

Fig. 11. Comparison of Performance Parameters for MOD 2.

shows output power spectrum for the whole system for 10 kHz frequency. MATLAB was used to read the output text file generated by WinSpice, and the data was processed using 1024-point FFT.

5. Simulation results

The proposed MASH 1-1 and MOD 2 modulators using GDI technique provide an improvement in the area, power, and Power Delay Product (PDP) as compared to standard CMOS technology. The delay remains the same for MOD 2 modulator whereas for MASH 1-1 modulator there is a slight increase in delay as compared to the CMOS technology. The area improvement is 24% for MASH 1-1 and 25% improvement for MOD 2. The power dissipation improvement is over 39% for MASH 1-1 and 24% improvement for MOD 2. Improvement in PDP is 15% for MASH 1-1 and 27% for MOD 2. The area, power, delay and PDP received are of modulator only, and it excludes DAC and LPF.

The performance parameters of digital modulators viz. SNDR (dB), SNR (dB), ENOB, and SFDR (dB) measured for both the modulators are represented graphically in the Figs. 10 and 11. respectively. Excess nodes and longer simulation time did not allow completion of readings for MASH 1-1 for 3 kHz frequency using CMOS technique.

6. Conclusion and future scope

This work proposes GDI based implementation of a sample 8-bit MASH 1-1 and MOD 2 modulators for audio frequencies. This work also proposes a full swing XOR gate in GDI technique which requires eight transistors less than the conventional CMOS technology. The proposed GDI technology based MASH 1-1 and MOD 2 modulators provide a significant improvement in the area, power dissipation, and PDP as compared to standard CMOS technology. The MOD 2 modulator consists of less GDI based gates hence less improvement in power dissipation is obtained as compared to MASH 1-1 modulator. However, there is 1.4 times increase in delay of MASH 1-1 modulator whereas, for MOD 2, there is no change in delay of GDI based technique as compared to those implemented in the standard CMOS technology. Due to no change in delay for MOD 2, the improvement in PDP is 27%, but for MASH 1-1 the improvement is 15%. The entire work uses audio frequency range, and comparison of the two methods show equal performance parameter measurement values of SNDR, SNR, SFDR, and ENOB. The same idea can be extended to high-resolution modulators and also to higher order digital modulators, where the reduction in area, delay, and PDP can be even greater.

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